Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-6 Canceled

7 (Currently Amended) A method of manufacturing a microelectronic device, comprising:

performing a first inspection of a device feature during an intermediate stage of manufacture;

cleaning the device feature after the first inspection; and

performing a second inspection of the device feature after cleaning the device feature, wherein the device feature is located in a production region of a wafer, the wafer further including a calibration region having a calibration feature located therein;

wherein the calibration feature comprises a first conductive layer located over the wafer, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer; and

wherein the first conductive layer comprises AlCu.

Claim 8. Canceled

9. (Currently Amended) The method of claim 8 wherein ~~the first conductive layer comprises AlCu,~~ the second conductive layer comprises W~~, and the buffer layer comprises:~~

~~a first TiN layer over the first conductive layer;~~

~~an implanted Ti layer over the first TiN layer; and~~

~~a second TiN layer over the implanted Ti layer~~.

Claims 10-22. Canceled

23. (Previously Presented) The method of claim 7 wherein at least one of the first and second inspections is performed by a scanning electron microscope (SEM).

24. (Previously Presented) The method of claim 7 wherein the cleaning comprises exposing the device feature to an oxygen containing plasma.

25. (Previously Presented) The method of claim 7 wherein the device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer.

26. (New) The method of claim 7 wherein the buffer layer comprises a first TiN layer over the first conductive layer, an implanted Ti layer over the first TiN layer, and a second TiN layer over the implanted Ti layer.

27. (New) A method of manufacturing a microelectronic device, comprising:

performing a first inspection of a device feature during an intermediate stage of manufacture;

cleaning the device feature after the first inspection; and

performing a second inspection of the device feature after cleaning the device feature, wherein the device feature is located in a production region of a wafer, the wafer further including a calibration region having a calibration feature located therein;

wherein the calibration feature comprises a first conductive layer located over the wafer, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer; and

wherein the second conductive layer comprises W.

28. (New) The method of claim 27 wherein the first conductive layer comprises AlCu.

29. (New) The method of claim 27 wherein the buffer layer comprises a first TiN layer over the first conductive layer, an implanted Ti layer over the first TiN layer, and a second TiN layer over the implanted Ti layer.

30. (New) The method of claim 27 wherein at least one of the first and second inspections is performed by a scanning electron microscope (SEM).

31. (New) The method of claim 27 wherein the cleaning comprises exposing the device feature to an oxygen containing plasma.

32. (New) The method of claim 27 wherein the device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer.

33. (New) A method of manufacturing a microelectronic device, comprising:

performing a first inspection of a device feature during an intermediate stage of manufacture;

cleaning the device feature after the first inspection; and

performing a second inspection of the device feature after cleaning the device feature, wherein the device feature is located in a production region of a wafer, the wafer further including a calibration region having a calibration feature located therein;

wherein the calibration feature comprises a first conductive layer located over the wafer, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer; and

wherein the buffer layer comprises a first TiN layer over the first conductive layer, an implanted Ti layer over the first TiN layer, and a second TiN layer over the implanted Ti layer.

34. (New) The method of claim 33 wherein the first conductive layer comprises AlCu.

35. (New) The method of claim 33 wherein the second conductive layer comprises W.

36. (New) The method of claim 33 wherein at least one of the first and second inspections is performed by a scanning electron microscope (SEM).

37. (New) The method of claim 33 wherein the cleaning comprises exposing the device feature to an oxygen containing plasma.

38. (New) The method of claim 33 wherein the device feature comprises a first conductive layer located over a substrate, a buffer layer located over the first conductive layer, and a second conductive layer located over the buffer layer.